PCB CONTROLLED IMPEDANCE, some simple notes.

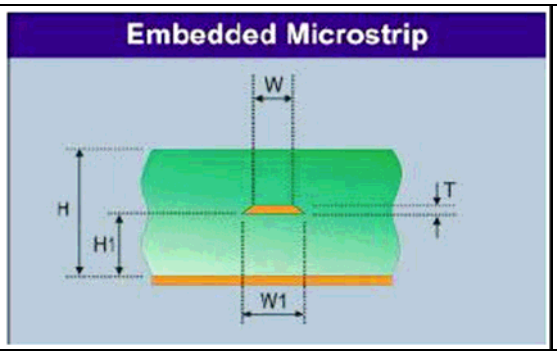
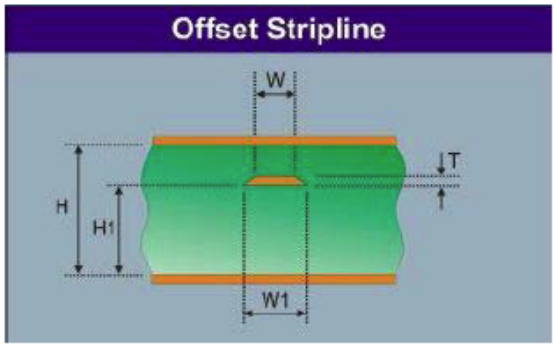
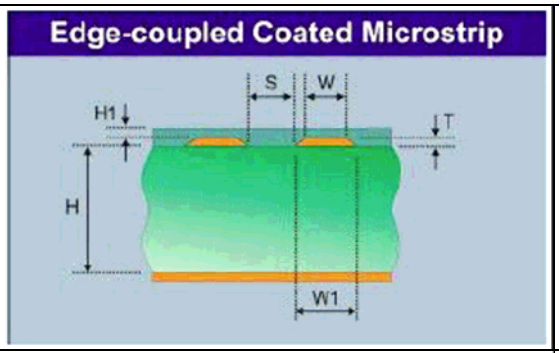
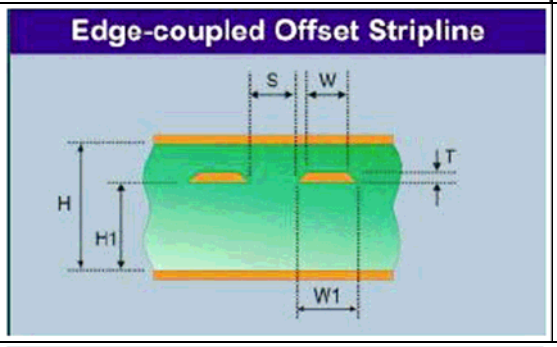
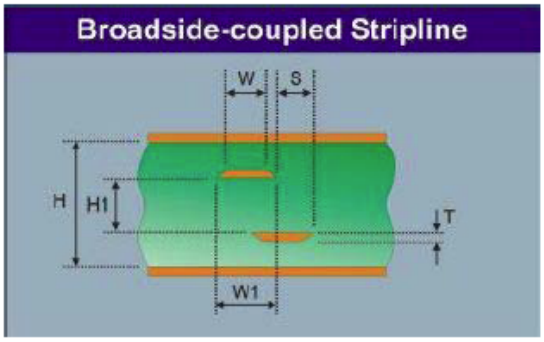
The antenna cable to a TV is most commonly coaxial; with an inner conductor insulated from the outer cylindrical conductor (shield). The dimensions of the conductors and insulator, and the electrical characteristics of the insulator are carefully controlled in order to determine the shape, strength and interaction of the electrical fields, and in turn the electrical impedance of the cable. Likewise many different trace configurations are used in the PCB industry to achieve controlled impedance.

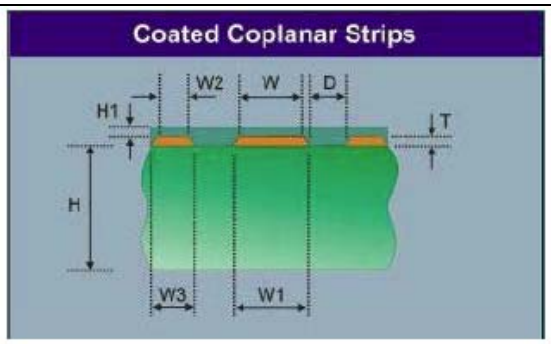
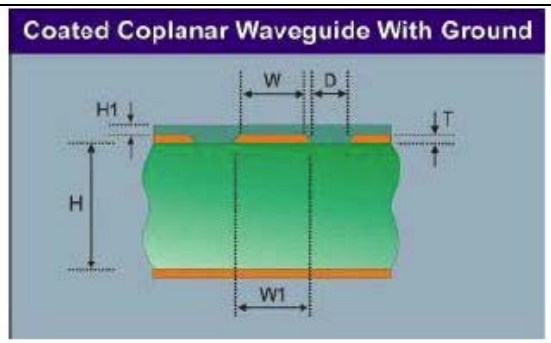
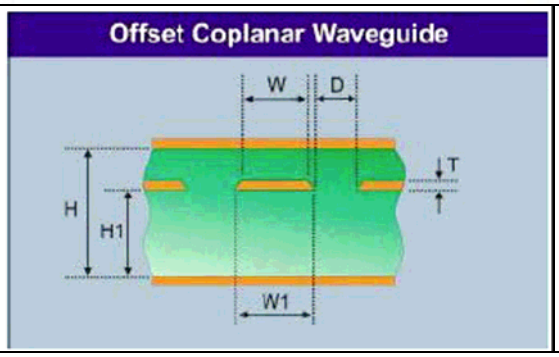
Controlled impedance PCB's emulate controlled impedance cables, where the coax shield may be represented by a Cu-plane, the insulator represented by the laminate and the conductor is the trace. As in a cable dimensions and materials determine the impedance.
These parameters must be carefully predicted in the design and controlled in the manufacturing process to ensure that specifications are met.
Impedance (measured in Ohms, Ω) is not to be confused with resistance (also Ohms, Ω). Resistance is a DC characteristic, while impedance is an AC characteristic of importance with increasing signal frequencies.

Coax Cable

Why do we need controlled impedances?
We need controlled impedances because the function of a wire or trace is to transfer signal power. Maximum signal power is achieved with matching impedances. The same considerations apply to signal transfer through traces on a PCB. When board traces carry high frequency signals, care must be taken to design traces matching the impedance of the driver and receiver devices. The longer the trace or the higher the frequencies, the higher is the need to control the trace impedance.
PCB manufacturers control impedance by varying the dimensions and spacing of the trace or laminate.
We at Elmatica experience an increase in demands for multilayers with controlled impedance. An estimated 80 % of the multilayer PCB's with eight layers or more are designed with controlled impedance.
In near future virtually all PCB's will likely include at least some impedance requirements. The following diagrams show some of the many configurations PCB designers can use. When looking at the stack-up of a multiplayer PCB, remember that controlled impedances are shielded by planes. For this reason you need only consider the laminate thicknesses between the planes on either side of the trace when it is inside the PCB.

These diagrams are examples of some of the many different configurations that PCB designers can use. When you are looking at the stack up of a multiplayer PCB, remember that controlled impedances are shielded by planes and for this reason, you only need consider the laminate thicknesses between the planes on either side of the trace when it is inside the PCB.

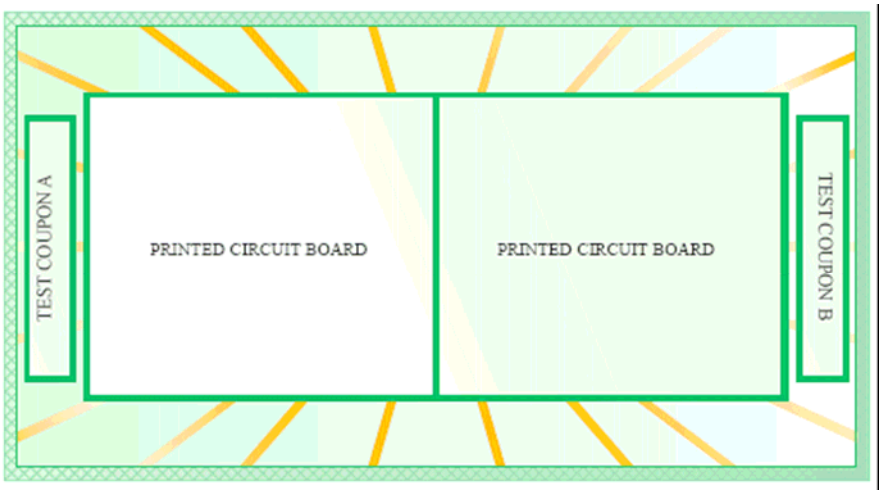
Embedded Microstrip contains a trace sandwiched within the PCB with a plane on one side and laminate and then air on the other.	
Offset Stripline contains a trace sandwiched within the PCB with a plane on both sides of the laminate.	
Edge coupled coated microstrip is a differentia lconfiguration where there are two controlled impedance traces on the surface, coated by resist and a plane on the other side of the laminate.	
Edge coupled offset Stripline is a differential configuration with two controlled impedance traces sandwiched between two planes. The traces are shown offset, however they could be midway between the planes (2H1+T=H).	
This differential configuration has two traces that are separated by laminate and sandwiched between two planes. Although the diagram shows the traces offset, the manufacturing objective is to have the traces with no offset, i.e. one should be directly above the other. Typically, this configuration is difficult to fabricate.	

In this Coated Coplanar Strips configuration, there is a single controlled impedance trace with two ground traces of a specified width (W2/W3) either side. All the traces are coated with resist.	
The Coplanar Waveguide has a single controlled impedance trace with planes either side (or very wide ground traces), a continuous plane on one side and laminate only on the other side.	
This Coplanar Waveguide is similar to the above configuration except that there are planes on both sides of the laminate as well as a plane on the same layer as the controlled impedance trace.	

…. And there are many more.

As the operating speed of electronic circuits has increased, so has the need for PCBs to have controlled impedances and the majority of PCB manufacturers are producing them.
As described earlier, if the value of controlled impedance is incorrect, it can be very difficult to identify the problem once the PCB is assembled. Since the impedance depends on many parameters (trace width, trace thickness, laminate thickness, etc.) the majority of PCBs are currently 100% tested for controlled impedance. However the testing is not normally performed on the actual PCB but on a test coupon manufactured at the same time and on the same panel as the PCB. Sometimes the test coupon is integrated into the main PCB.

But, on most PCBs, the impedance is calculated during pre-production, and not controlled through use of coupons. General tolerance on the impedance is +/- 10%.



Typical Production Panel

- *It is rare for controlled impedance traces to be easily accessible for testing (including a closely situated ground connection).*
- *Planes are not interconnected on the main PCB and this may lead to inaccurate measurements.*
- *Accurate and consistent testing results require a straight single trace of 150mm (or longer), often the actual PCB trace is shorter than 150mm.*
- *The actual PCB trace may have branches or vias which makes accurate measurement very difficult*
- *Adding extra pads and vias for testing on the PCB will affect the performance of the controlled impedance trace and will occupy space needed for the function of the PCB.*

The typical test coupon is a PCB approximately 200x30mm with exactly the same layer and trace construction as the main PCB. It has traces that are designed to be the same width and on the same layer as the controlled impedance traces on the main PCB.

When the artwork is produced, the same aperture code (D-code) used for the controlled impedance traces is used to produce the test traces on the coupon. Since the coupon is fabricated at the same time as the main PCB the coupon's traces will have the same impedance as those on the main PCB. All planes are included on the coupon and they are interconnected on the coupon only, to ensure that test results are valid. It is necessary to include a void around the coupon on the reference planes so as not to affect the connectivity of the PCB itself if BBT (BareBoard Test) occurs whilst still on the panel

Usually one coupon is made at the end of each panel to ensure that the coupon is representative of the whole panel. I.e. testing the 2 coupons will verify to a high confidence level that there are no differences in trace width, trace thickness, laminate height, etc. over the whole panel.

In addition to the usual PCB specifications, the PCB designer should specify:

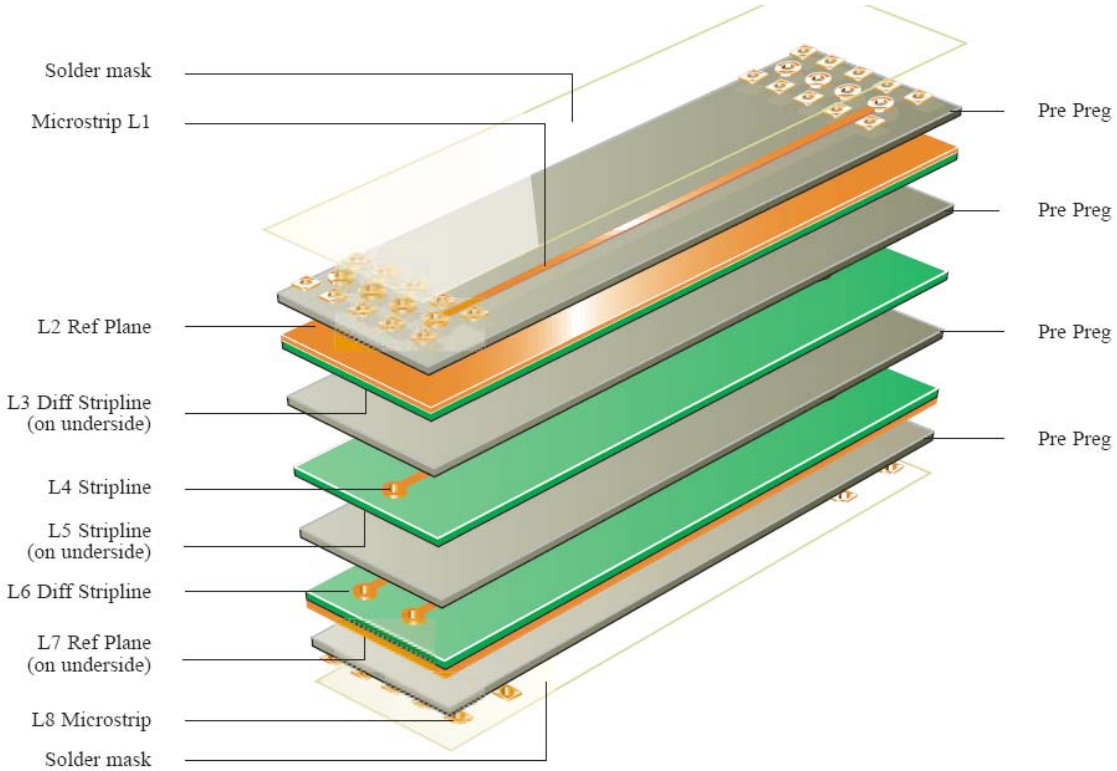
- Which layers contain controlled impedance traces

- The impedance(s) of the trace(s) (there can be more than one value of impedance trace per layer)
- Separate aperture codes for controlled impedance traces e.g. 4 mil non controlled impedance trace and 4 mil controlled impedance trace.
- And either:
  1. the width (w) of the controlled impedance trace or
  2. the laminate thickness (h) adjacent to the controlled impedance trace.

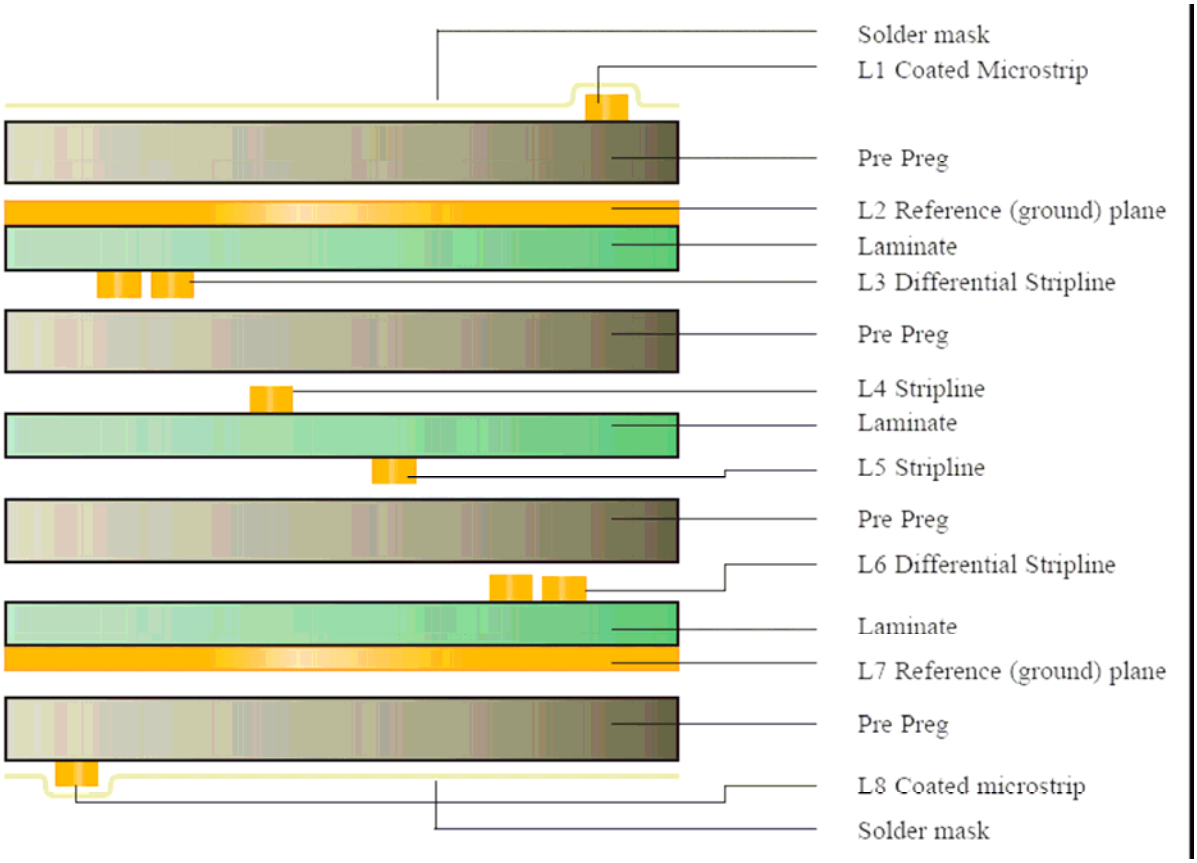
In case 1, where trace width (w) is specified, the manufacturer will adjust the laminate thick-ness (h) to give the correct value of impedance.

In case 2 where the laminate thickness (h) is specified, the manufacturer will adjust the trace width (w) to achieve the value of impedance.

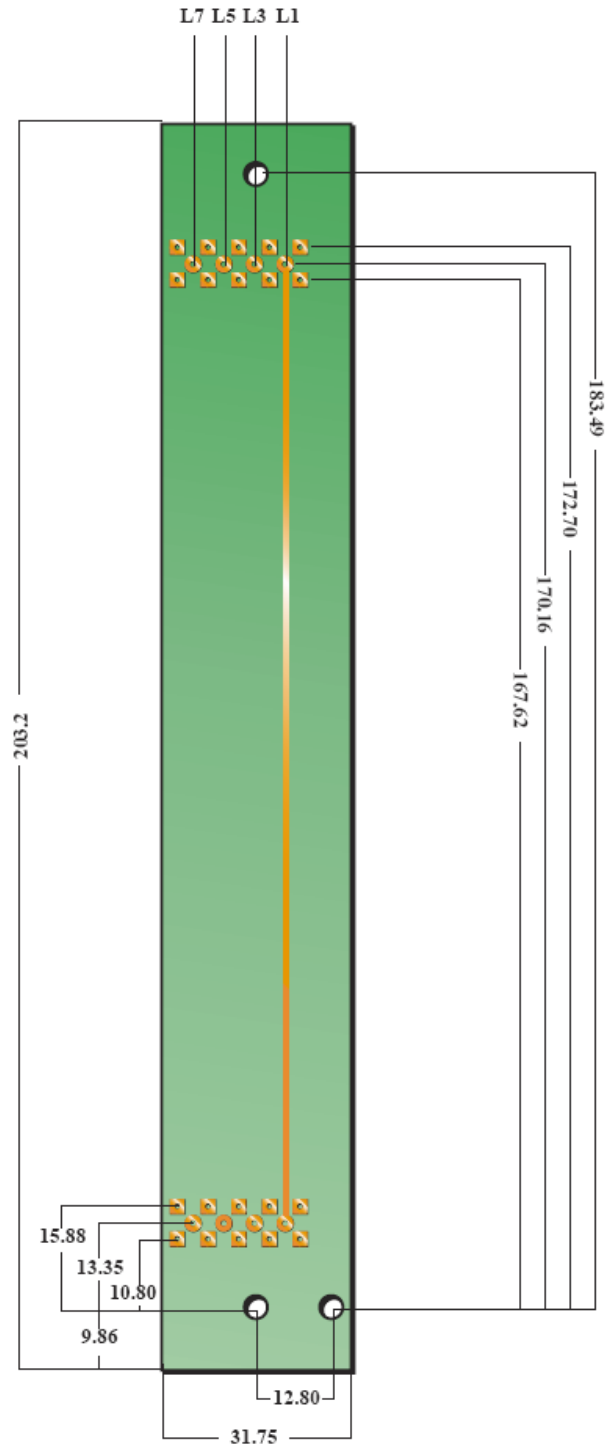
Some configurations (differential, coplanar) may have more than one parameter that can be varied to obtain the specified impedance.

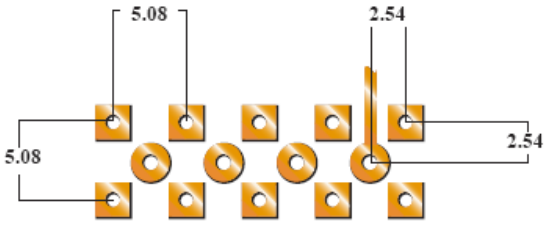


Exploded view of a test coupon 1



Exploded view of a test coupon 2





not to scale

Typical Test Coupon

(Reference IEC draft, addition to IEC326-3)

1. Dielectric separation will replicate impedance structure on printed boards.
2. Test connection holes shall be plated through to access all inner layer test conductors.
3. Square pads identify plated through hole connections to access all ground/power reference planes.
4. Conductor widths will replicate critical conductors on each impedance layer.
5. Via holes to be added as required.
6. Cross hatching to be added to outer layer as required.
7. Two coupons per panel. These to be individually identified with letter A& B respectively.
8. Job No. + Date code to be added as per customer requirements.
9. All planes to be interconnected (on test coupon only).

Capacitive loading

To minimise capacitive loading during test, you should minimise the size of pads and vias on coupons, especially for high impedance traces. Although this standard coupon design shows pads at both ends, you are likely to obtain better test results on high impedance traces if you only place a pad at one end.

Note that you can download Gerber files for a typical impedance test coupon from www.elmatica.no.

Simple DESIGN GUIDELINES.

The following guidelines should be used for designing and specifying differential stripline configurations:

- No special fabrication requirements are required for differential transmission lines.
- A higher tolerance will be required when the differential lines are on adjacent layers that are separated by prepreg.
- Broadside-coupled striplines should ideally be used on a core. Try to avoid having prepreg between them. This is required to control the z-axis alignment between the two signal layers.
- Specify the design trace-to-trace spacing for correct impedance modelling.
- Your manufacturer should be involved in the pre-layout phase to assist with the line width and spacing calculations.
- Give the differential pairs a different aperture than non-differential traces. This will make it easier for the manufacturer to adjust line widths during the tooling process.

MINIMIZING IMPEDANCE COST

Using the following simple guidelines will reduce the cost impact when specifying controlled impedance PCB's:

- Only specify the impedance on the layers where it is actually required.
- Route all of the controlled impedance traces onto the same layers.
- Specify a +/- 10% tolerance when possible.
- Do not specify all of the physical dimensions for the trace. Just specify the required impedance and allow the manufacturer to determine the physical parameters. Try to just specify the trace width and tolerance based on the PCB routing.
- Do not require impedance test coupons. This may reduce the panel utilization and will require each PCB to be manually tested. Impedance will be calculated with the values set by the manufacturer.
- Allow panel level testing, without individual PCB serialization, to verify the PCB impedance. Panel testing has been shown to provide sufficient results comparable to individual PCB testing.

Elmatica source for PCB Controlled Impedance is as it is for the rest of the PCB business, www.polarinstruments.com *josse Dec. 2008*